Kindly add new claim 219 as follows:

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219. (New) The method of claim 68 wherein first memory location and the second memory location comprise the same memory location.

REMARKS

The amendments to claim 1 are supported by the embodiments described in connection with Figs. 3 and 6, page 28, line 3 through page 30, line 16 and page 31, line 33 through page 33, line 11. New claim 219 is supported by the embodiments described in connection with Fig. 18 at page 47, line 25 to page 49, line 20.

In summary, each of claims 1, 3-9, 17-22 and 24-219 is allowable, and such action is respectfully requested.

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Respectfully submitted,

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Version of Amended Claims With Markings To Show Changes Made
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1. (Amended) A memory module [,] comprising:

a. a memory cell having a memory state; [and]

b. a local sense amplifier coupled with the memory cell, the local sense amplifier sensing the memory state and producing a local memory state signal representative thereof [, wherein the local sense amplifier produces a limited swing voltage signal];

c. a global sense amplifier coupled with the local sense amplifier, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof;

d. a local wordline decoder coupled with the memory cell, the local wordline decoder generating a local memory cell selection signal in response to a local decoder selection signal; and

e. a global wordline decoder coupled with the local wordline decoder, the global wordline decoder producing the local decoder selection signal responsive to a global selection signal, at least two of the local memory state signal, global memory state signal, local decoder selection signal and global selection signal comprise a limited swing voltage signal.

4. (Amended) The memory module of claim 3, further comprising [:

a. a plurality of local sense amplifiers [; and

b. a] wherein the global sense amplifier [,] is coupled with the plurality of local sense amplifiers, a selected one of the plurality of local sense amplifiers sensing the memory state and producing a local memory state signal representative thereof, the global sense amplifier sensing the local memory state signal and producing a global memory state signal representative thereof, and wherein the plurality of memory cells coupled with the global sense amplifier is disposed as a memory column.

8. (Amended) The memory module of Claim 1, wherein at least three of the local memory state signal, global memory state signal, local decoder selection signal and global selection signal comprise a limited swing voltage signal [the local sense amplifier is responsive to a limited swing voltage signal from the memory cell representative of the memory state].

9. (Amended) The memory module of Claim [2] 1, wherein each of the local memory state signal, global memory state signal, local decoder selection signal and global selection signal comprises a limited swing voltage signal [the global sense amplifier is responsive to a limited swing voltage signal representative of the memory state].

18. (Amended) The memory module of Claim 17, [further comprising a] wherein the global wordline decoder is coupled with the plurality of local wordline decoders, the global wordline decoder producing the local decoder selection signal

responsive to [a] the global selection signal, and wherein the plurality of memory cells coupled with the global wordline decoder is disposed as a memory row.

20. (Amended) The memory module of Claim 7, further comprising a plurality of local wordline decoders coupled with respective memory cells, selected ones of the plurality of local wordline decoders selecting respective memory cells responsive to a corresponding local decoder selection signal.

21. (Amended) The memory module of claim 20, further comprising a global wordline decoder coupled with the plurality of local wordline decoders, the global wordline decoder producing the local decoder selection signal responsive to a global selection signal, and wherein the plurality of memory cells coupled with the global wordline decoder is disposed as a memory row.

35. (Amended) The memory module of claim 25, wherein the wordline decoder includes a selection signal input, and further comprises [comprises] a multiplexer operably coupled with the first memory row and the second memory row, the multiplexer selectably directing the local selection signal from the wordline decoder selection signal input to the selected one of the first memory row and the second memory row.

37. (Amended) The memory module of Claim [12] 1, further comprising a high-precision delay measurement circuit constraining the limited swing voltage [swing] signal.

43. (Amended) The memory module of Claim [23] 1, further comprising a high-precision delay measurement circuit constraining the limited swing voltage [swing] signal.

49. (Amended) The memory module of Claim [23] 1, further comprising a diffusion replica delay circuit constraining the limited swing voltage [swing] signal.

52. (Amended) The memory module of Claim [2] 1, further comprising a data transfer bus circuit coupling the global sense amplifier to a data bus.

58. (Amended) The memory module of Claim 22, wherein one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders comprises a limited swing voltage circuit, the limited swing voltage circuit producing a limited swing voltage signal of a respective one of the global memory state signal, the local memory state signal, the global selection signal, and the local decoder selection signal.